A red and white logo

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**ECE 524   
Instructor: Philip Tracton  
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**Verification Document   
for  
Implementing Neural Network in Zybo z10 Board using VHDL**

**by:**

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1. **Introduction**

This document presents the strategy for verification of the FPGA Classification System for Fashion MNIST. It also explains the testing mechanism and provides proof of satisfying all requirements mentioned in the specification document via the self-checking test bench provided.

1. **Requirements Verification**

**2.1 System Initialization (REQ-SYS-1, REQ-TOP-1)**

**Verification Method:** The testbench initializes the system by asserting the reset signal:

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**Evidence of Compliance:** The testbench confirms proper initialization**:**

**A white rectangle with black text

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* 1. **UART Communication (REQ-SYS-2, REQ-UART-1)**

**Verification Method:** The testbench transmits all 784 pixels of the test image via UART:

**A screenshot of a computer program

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**Evidence of Compliance:** The testbench confirms successful UART communication:

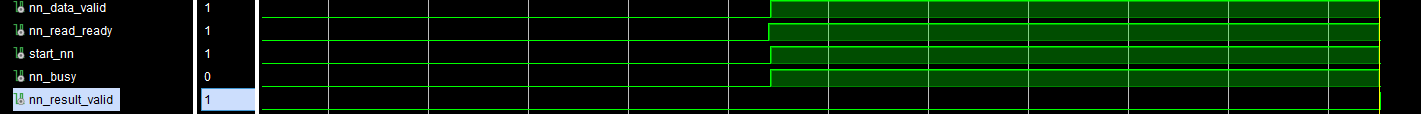
**A screen shot of a computer program

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* 1. **Neural Network Processing (REQ-SYS-3, REQ-NN-1, REQ-NN-3, REQ-MLP-1)**

**Verification Method:** The testbench initializes the system by asserting signals like nn\_data\_valid , nn\_read\_ready,nn\_busy, result\_valid, data\_out\_valid

**Evidence of Compliance**: The testbench confirms successful neural network processing:



A close-up of a computer screen

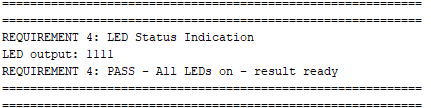
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* 1. **LED Status Verification (REQ-SYS-4, REQ-TOP-2, REQ-TOP-3)**

**Verification Method:** The testbench monitors LED status changes throughout the processing sequence and verifies the final LED state.

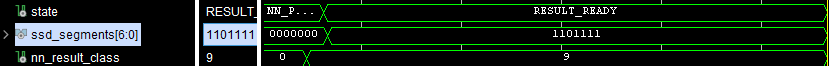
**Evidence of Compliance**: The testbench confirms correct LED status indication.



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* 1. **Classification Output (REQ-TOP-4, REQ-NN-2)**

**Verification Method:** The testbench checks the seven-segment display pattern for the correct class.

**Evidence of Compliance:** The testbench confirms correct classification display:

A close-up of a card

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* 1. **Image storage (REQ-BRAM-1)**

**Verification Method:** The testbench has signals like bram\_write\_addr, bram\_write\_en for Image storing.

**Evidence of Compliance:** The testbench confirms image storing in the BRAM.



* 1. **Clock generation and Crossing Verification (REQ-BRAM-2, REQ-CLK-1)**

**Verification Method:** The testbench has waveforms for 125 MHZ and 36MHZ clock to verify the clock generation and crossing.

**Evidence of Compliance:** The testbench waveform of both clocks .125MHZ clock has 8ns wave and 36 MHZ has ~28 ns wave.

